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Describes the features and functions of the Arm® Cortex® -A9 and peripherals contained in the hard processor system. ... Intel Arria 10 Hard Processor System Technical Reference Manual. Intel Arria 10 Hard Processor System Technical Reference Manual Revision History; Introduction to the Hard Processor System.

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• Cortex™ -A9 Technical Reference Manual (ARM DDI 0388) • Cortex-A9 MPCore Technical Reference Manual (ARM DDI 0407) • Cortex-A9 Configuration and Sign-Off Guide (ARM DII 0146) • AMBA AXI Protocol Specification (ARM IHI 0022) • ARM Architecture Reference Manual, ARMv7-A and ARMv7-R edition (ARM DDI 0406).

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Cortex-A9 Technical Reference Manual . Preface: Introduction; Functional Description; Programmers Model; The System Control Coprocessors; Memory Management Unit; Level 1 Memory System; Level 2 Memory Interface; Preload Engine; Performance Monitoring Unit; Debug. About the debug interface; About the Cortex-A9 debug interface; Debug register ...

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This preface introduces the Cortex-A9 MBIST Controller Technical Reference Manual. ... In this book, the generic term MBIST controller means the Cortex-A9 MBIST controller, and Cortex-A9 processor means the Cortex-A9 processor family. Product revision status The r n p n identifier indicates the revision status of the product described in this manual.

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Cortex-A9 Technical Reference Manual . Preface: Introduction; Functional Description; Programmers Model. About the programmers model; ThumbEE architecture; The Jazelle Extension; Advanced SIMD architecture; Security Extensions architecture; Multiprocessing Extensions; Modes of operation and execution; Memory model; Addresses in the Cortex-A9 ...

[Cortex-A9 Technical Reference Manual - ARM architecture](#)
The Technical Reference Manual (TRM) describes the functionality and the effects of functional options on the behavior of the Cortex-A9 family of processors. the Cortex-A9 TRM describes the uniprocessor variant. the Cortex-A9 MPCore TRM describes the multiprocessor variant of the Cortex-A9 processor.

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